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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]This invention relates to a solid state camera. Especially this invention relates to the solid state camera which has a high-intensity correcting function. Furthermore, this invention relates to the solid state camera which has a high-intensity correcting function which can realize a miniaturization and can realize improvement in the speed of working speed.
[0002]
[Description of the Prior Art]A solid state camera (CMOS sensor) is provided with a picture element region (light sensing portion), a horizontal line memory circuit, a horizontal shift register circuit, a vertical shift register circuit, and an output amplifier circuit. A picture element region is formed by the pixel by which was horizontal and multiple arrays were carried out perpendicularly (to matrix form). A pixel is equipped with the optoelectric transducer (photo-diode) which changes a lightwave signal into an electrical signal. The predetermined pixel of a picture element region is chosen by the vertical shift register circuit, and the pixel signal accumulated in this selected pixel is memorized in a horizontal line memory circuit. The pixel signal of the selected pixel and the pixel arranged in the same horizontal line is memorized similarly in a horizontal line memory circuit. Two or more pixel signals of the same horizontal line memorized in the horizontal line memory circuit are transmitted to an output amplifier circuit one by one in a horizontal shift register circuit. An output amplifier circuit amplifies a pixel signal and this amplified pixel signal is outputted to the exterior of a solid state camera. After the pixel signal of the pixel arranged in 1 horizontal line is read, the pixel signal of the pixel arranged in 1 horizontal line of the next step is read.
[0003]These days, the research and development which include a part of high-intensity correcting function in a solid state camera are furthered. A high-intensity correcting function is a function to correct a picture which is saturated by photography in the state where the light of a fluorescent lamp enters in the photography and the interior of a room in the state where sunlight enters in outdoor.
[0004]It is necessary to generate the high luminance correction signal (highlight correcting signal) for amending high-intensity in realization of a high-intensity correcting function, and to correct a pixel signal to it with a high luminance correction signal. In the solid state camera which has a high-intensity correcting function which this invention person is developing, Two pixels (two horizontal lines) from which the exposure time of a picture element region differs were chosen, and the method which takes out the pixel signal of one of other pixels as a high luminance correction signal was adopted as a regular signal for the pixel signal of

one pixel to generate a picture. A pixel signal is a signal generated by the prolonged exposure time equivalent to about 1 frame period which makes the picture of one sheet. A high luminance correction signal is a signal which was taken out from the pixel and generated by short-time exposure time compared with the pixel signal, after a pixel signal is taken out from a pixel and the horizontal scanning of a number - ten numbers is performed.

[0005]A pixel signal and a high luminance correction signal are outputted from a solid state camera that it is simultaneous and in parallel for every horizontal line, respectively. As above-mentioned, the pixel of 1 horizontal line is chosen by the vertical shift register circuit, and the pixel signal which is a pixel of this 1 horizontal line is memorized in a horizontal line memory circuit. The pixel signal memorized in this horizontal line memory circuit is outputted to an external device through an output amplifier circuit. the high luminance correction signal separately allocated with the horizontal line memory circuit where the same circuitry also as the output of a high luminance correction signal is required, and a high luminance correction signal memorizes a pixel signal -- service water -- it memorizes in a common line memory circuit. furthermore -- a vertical shift register circuit and a horizontal shift register circuit are separately allocated for the output of a high luminance correction signal -- a high luminance correction signal -- service water -- the high luminance correction signal memorized in the common line memory circuit is outputted outside through the output amplifier circuit allocated separately.

[0006]The pixel signal outputted to the exterior of the solid state camera lets each of the auto gain controller device and analog to digital converter device by which external was carried out pass one by one, and is once memorized by the frame memory device. In alternative pathway, the high luminance correction signal outputted to the exterior of the solid state camera passes an auto gain controller device and an analog to digital converter device one by one, and is once remembered to be a processor of a pixel signal by the frame memory device allocated separately. The pixel signal memorized by the frame memory device and the high luminance correction signal memorized by other frame memory devices are outputted to a synthesizer unit, respectively, and a synthesizer unit corrects a pixel signal based on a high luminance correction signal.

[0007]

[Problem(s) to be Solved by the Invention]In the above-mentioned solid state camera, consideration is not made about the following points.

[0008](1) 1 set of peripheral circuits which include a horizontal shift register circuit, a vertical shift register circuit, a horizontal line memory circuit, and an output amplifier circuit in a solid state camera -- in addition, 1 set of other peripheral circuits which have equivalent circuitry which builds a high-intensity correcting function are allocated. In order to have 2 sets of peripheral circuits which have an equivalent function, a solid state camera becomes large-sized. A solid state camera comprises a sealed body (package) which generally closes a semiconductor chip (semiconductor substrate in which various circuits were formed), and this semiconductor chip, and a sealed body becomes large-sized while a semiconductor chip becomes large-sized.

[0009](2) the external terminal (an outer lead or an outer pin) which outputs a pixel signal to a solid state camera -- in addition, the external terminal which outputs a high luminance correction signal is needed separately. The increase in the number of external terminals enlarges a solid state camera.

[0010](3) In order to reduce the number of external terminals, in equipping a solid state camera with an output switching circuit and outputting a pixel signal and a high luminance correction signal from one external

terminal, the signal quantity for 1 horizontal line turns into signal quantity which applied the signal quantity of the high luminance correction signal to the signal quantity of a pixel signal, and a data rate increases. According to increase of this data rate, since the output time of the pixel signal for one frame becomes long, the working speed of a solid state camera becomes slow as a result.

[0011](4) Since each of two kinds of pixel signals and a high luminance correction signal is outputted from a solid state camera, 2 sets of each of an auto gain controller device, an analog to digital converter device, and a frame memory device are needed for the external external device of a solid state camera, and a concrete target. Therefore, the wiring board which mounts a solid state camera and an external device is enlarged, and the camera incorporating a solid state camera itself becomes large-sized.

[0012](5 In a solid state camera, it is necessary to adjust the signal quantity of a high luminance correction signal according to the picture demanded on a user side, and to adjust a dynamic range further.) Regulation of the signal quantity of a high luminance correction signal can be carried out by adjusting regulation of the exposure time of a pixel, i.e., the pixel number between the pixel which takes out a pixel signal, and the pixel which takes out a high luminance correction signal, (horizontal line number). However, in addition to regulation of the signal quantity of the high luminance correction signal by the side of such a solid state camera, the contents of processing of the external device also needed to be adjusted, and regulation of the dynamic range was dramatically difficult.

[0013]This invention is made in order to solve an aforementioned problem. Therefore, the purpose of this invention is to provide the solid state camera which reduces the number of external terminals and can realize miniaturization and integration. Especially this invention realizes the miniaturization of a solid state camera, and an object of this invention is to attain the miniaturization of mounting devices, such as a camera which mounts this solid state camera.

[0014]The purpose of this invention is to provide the solid state camera which reduces the data rates of a pixel signal and can realize improvement in the speed of the output operation speed of a pixel signal.

[0015]The purpose of this invention is to provide the solid state camera which can adjust the signal quantity of a high luminance correction signal simply, and a dynamic range can control easily.

[0016]

[Means for Solving the Problem]In order to solve an aforementioned problem, this invention equips a solid state camera with the following.

A picture element region where a pixel which accumulates a pixel signal was arranged by multi-line seriate.

A pixel signal storing memory circuit which memorizes temporarily a pixel signal accumulated by a predetermined pixel of a picture element region.

A high luminance correction signal storing memory circuit which memorizes temporarily a high luminance correction signal which amends high-intensity [which was accumulated by the same predetermined pixel], A synthetic circuit which outputs a pixel signal which compounded a high luminance correction signal memorized in a pixel signal memorized in a pixel signal storing memory circuit, and a high luminance correction signal storing memory circuit, and with which high-intensity was amended.

[0017]A pixel signal accumulated by a predetermined pixel is accumulated by long exposure time equivalent to a part for 1 frame period which generates a picture of about one sheet. A pixel signal is read and a high luminance correction signal accumulated by the same predetermined pixel is accumulated by short exposure

time after a horizontal scanning of a number - the number of ten lines set up beforehand was carried out.
[0018]In a pixel signal storing memory circuit, a storage cell of the number (it responded to the region of accommodation of a dynamic range) according to the number of times of a horizontal scanning beforehand set as a direction of transfer of a pixel signal and a high luminance correction signal is arranged in in-series. A pixel signal transmitted from a predetermined pixel is once memorized in a high luminance correction signal storing memory circuit. A pixel signal which a pixel signal transmitted from a pixel of the next step of a predetermined pixel was memorized in a high luminance correction signal storing memory circuit when a horizontal scanning for 1 horizontal line was completed, and was first memorized by this storage operation in a high luminance correction signal storing memory circuit is transmitted to a pixel signal storing memory circuit, and is memorized. In a pixel signal storing memory circuit, according to the number of times of a horizontal scanning set up beforehand, two or more storage cells are perpendicularly arranged in in-series, and a pixel signal is transmitted to this storage cell one by one.
[0019]A memory shift register circuit and a line selecting circuit are connected to a pixel signal storing memory circuit, respectively. A memory shift register circuit transmits a pixel signal inputted into a pixel signal storing memory circuit one after another one by one to a storage cell arranged perpendicularly. A line selecting circuit takes out a picture signal corresponding to a predetermined pixel memorized in a pixel signal storing memory circuit, and this pixel signal is transmitted to a synthetic circuit.
[0020]A horizontal shift register circuit shared by each is connected to a pixel signal storing memory circuit and a high luminance correction signal storing memory circuit. A horizontal shift register circuit transmits a pixel signal memorized in a pixel signal storing memory circuit to a synthetic circuit through a line selecting circuit. A level shift resist circuit transmits a high luminance correction signal memorized in a high luminance correction signal storing memory circuit to a synthetic circuit.
[0021]Each of a horizontal shift register circuit, a line selecting circuit, and a synthetic circuit is connected to a controller circuit. A controller circuit controls a line selecting circuit and takes out a pixel signal memorized in a pixel signal storing memory circuit. A control circuit controls a synthetic circuit and performs composition with a high luminance correction signal memorized in a pixel signal memorized in a pixel signal storing memory circuit, and a high luminance correction signal storing memory circuit.
[0022]These picture element regions, a pixel signal storing memory circuit, a high luminance correction signal storing memory circuit, a horizontal shift register circuit, a synthetic circuit, a memory shift register circuit, a line selecting circuit, and an output amplifier circuit are integrated by one semiconductor substrate (1 chip making is carried out).
[0023]In a solid state camera constituted in this way, a pixel signal and a high luminance correction signal are taken out from the same predetermined pixel of a picture element region, a pixel signal is memorized in a pixel signal storing memory circuit, and a high luminance correction signal is memorized in a high luminance correction signal storing memory circuit. Since a high luminance correction signal storing memory circuit is arranged between a picture element region and a pixel signal storing memory circuit and these signals are perpendicularly transmitted in order of a pixel signal and a high luminance correction signal, memory of a pixel signal and memory of a high luminance correction signal are performed to the same timing. Each of a pixel signal and a high luminance correction signal which were memorized is transmitted to a synthetic circuit in a common horizontal shift register circuit. Therefore, since a horizontal shift register circuit to which only a high luminance correction signal is transmitted becomes unnecessary and a common horizontal shift register

circuit is allocated in a pixel signal storing memory circuit and a high luminance correction signal storing memory circuit, The number of horizontal shift register circuits can be reduced, and a miniaturization of a solid state camera and integration can be realized.

[0024]A synthetic circuit is allocated in a solid state camera, and correction of a pixel signal is made inside a solid state camera. That is, a pixel signal outputted from a solid state camera will be one kind of a pixel signal with which high-intensity was amended. Therefore, since the number of external terminals (pin) of a solid state camera is reducible, a miniaturization of a solid state camera and integration (or reduction of package size) are realizable.

[0025]Since regulation of signal quantity of a high luminance correction signal can be substantially performed only by the solid state camera side, regulation of an external device becomes unnecessary and can adjust a high luminance correction signal easily.

[0026]A pixel signal acquired by the same predetermined pixel of a picture element region in a solid state camera, Each of a high luminance correction signal is serially transmitted to each of a high luminance correction signal storing memory circuit and a pixel signal storing memory circuit one by one, and extraction by a pixel signal and a high luminance correction signal by a synthetic circuit is performed to the same timing. Therefore, since circuit systems for compounding a pixel signal and a high luminance correction signal are reducible to 1 set, a miniaturization of a solid state camera is realizable.

[0027]In a solid state camera, a circuit system for compounding a pixel signal and a high luminance correction signal as mentioned above can reduce to 1 set, and since one kind of output may be sufficient as a pixel signal with which high-intensity was amended, a data rate of a pixel signal is shortened. Time which an output of a pixel signal for 1 frame period takes by shortening of a data rate of a pixel signal can be shortened (halved), and working speed of a solid state camera can be accelerated.

[0028]

[Embodiment of the Invention]Hereafter, an embodiment of the invention is described.

[0029]Drawing 1 is a flat-surface layout pattern of the solid state camera concerning an embodiment of the invention. As shown in drawing 1, the solid state camera 1, A picture element region. (Light sensing portion) 2 A vertical shift register circuit. (VSR) 3, 4, the vertical shift register switch circuit 9, 1 horizontal line memory circuit 6, the column type auto gain controller circuit (AGC) 7, the column type analog to digital converter circuit (ADC) 8, the high luminance correction signal storing memory circuit 10, the pixel signal storing memory circuit 11, It has the memory shift register circuit 12, the line selecting circuit (LS) 13, the synthetic circuit 14, the horizontal shift register circuit (HSR) 15, and the output amplifier circuit 16, and is built. That is, the solid state camera 1 integrates and carries out 1 chip making of these picture element regions 2 and the various peripheral circuits of those to one semiconductor substrate.

[0030]The picture element region 2 of the solid state camera 1 arranges two or more pixels P11, P12, --, P1n, --, Pmn to matrix form to horizontal and a perpendicular direction, and is constituted. For example, in the solid state camera 1 concerning this embodiment, a VGA format is made in the picture element region 2, in about 700 pixels P arranged horizontally, about 640 pieces are used as an effective pixel, and the remainder is used as dummy pixels. In about 500 pixels P arranged perpendicularly, about 480 pieces are used as an effective pixel, and the remainder is used as dummy pixels. Each pixel P11-Pmn is provided with the optoelectric transducer at least, changes a lightwave signal into an electrical signal, and generates a pixel signal. The pixels P11-Pmn generate a high luminance correction signal.

[0031]Drawing 2 is a representative circuit schematic (the equivalent circuit of a peripheral circuit is also shown in part.) of the suitable pixel for this embodiment. The one pixel P is arranged at each crossing portion of address signal line ADL, the reset signal wire RSL, the video signal line 6L, and the reset signal supply lines RL. As shown in drawing 1 and drawing 2, address signal line ADL is connected to each of the vertical shift register circuits 3 and 4 via the vertical shift register switch circuit 9. Similarly, the reset signal wire RSL is connected to each of the vertical shift register circuits 3 and 4 via the vertical shift register switch circuit 9. The vertical shift register switch circuit 9 arranges two or more OR circuits, and is constituted.

[0032]When the vertical shift register circuit 3 is chosen by the vertical shift register switch circuit 9, in order that address signal line ADL may read a pixel signal, the pixel P is chosen, and the reset signal wire RSL chooses the pixel P, in order to perform a reset action. This selection is performed about all the pixels P arranged in the same horizontal line.

[0033]When the vertical shift register circuit 4 is chosen by the vertical shift register switch circuit 9, in order that the same address signal line ADL may read a high luminance correction signal, the pixel P is chosen, and the reset signal wire RSL chooses the pixel P, in order to perform a reset action. This selection is performed about all the pixels P arranged similarly in the same horizontal line.

[0034]The video signal line 6L is connected to 1 horizontal line memory circuit 6, and the pixel signal and high luminance correction signal of the pixel P are transmitted to 1 horizontal line memory circuit 6 through the video signal line 6L. The picture signal accumulated in two or more pixels P (for example, pixel P11-P1n) arranged in one horizontal line is transmitted to 1 horizontal line memory circuit 6 in parallel, and each pixel signal is memorized temporarily in 1 horizontal line memory circuit 6. The reset signal supply lines RL are chosen in the case of the reset action of the pixel P, and supply reset potential. The reset signal supply lines RL supply the drain potential of MISFET for addresses (T3) simultaneously.

[0035]The pixel P Optoelectric-transducer PD, It has MISFET(Metal Insulator Semiconductor Field Effect Transistor) T1 for signal amplification, MISFETT2 for reset, MISFETT3 for address signals, and the signal detection part S, and is constituted. The pixel P concerning this embodiment comprises an amplified type pixel which amplifies the pixel signal (or high luminance correction signal) acquired by optoelectric-transducer PD by MISFETT1 for signal amplification.

[0036]Optoelectric-transducer PD is formed with the photo-diode which consists of pn junction, and changes a lightwave signal into an electrical signal. The electrons by which photoelectric conversion was carried out are collected by optoelectric-transducer PD, and change the potential of the signal detection part S which is a n type region of pn junction. The signal detection part S is connected to the gate electrode of MISFETT1 for signal amplification.

[0037]MISFETT1 for signal amplification connects the source region to the video signal line 6L, and it connects a drain area to the source region of MISFETT3 for address signals. MISFETT1 for signal amplification amplifies the pixel signal (or high luminance correction signal) of the signal detection part S, and it outputs the amplified pixel signal to the video signal line 6L.

[0038]MISFETT3 for address signals connects a gate electrode to address signal line ADL, it connects the source region to the video signal line 6L, and connects a drain area to the reset signal supply lines RL.

[0039]MISFETT2 for reset connects the source region to the signal detection part S, it connects a drain area to the reset signal supply lines RL, and connects a gate electrode to the reset signal wire RSL.

[0040]Each of MISFETT1 for signal amplification which constitutes these pixels P, MISFETT2 for reset, and

MISFETT3 for address signals comprises n channel MISFET.

[0041]In the read operation of a pixel signal, the vertical shift register circuit 3 scans sequentially and chooses perpendicularly the pixel P arranged in the picture element region 2, as shown in drawing 1. The vertical shift register circuit 4 scans sequentially and chooses perpendicularly the pixel P arranged in the picture element region 2 in the read operation of a high luminance correction signal. The scan of the vertical shift register circuit 4 is performed by continuing after the scan by the vertical shift register circuit 3 according to the signal quantity of a high luminance correction signal.

[0042]The column type auto gain controller circuit 7 shown in drawing 1 performs gain control of the pixel signal (analog signal) memorized temporarily in 1 horizontal line memory circuit 6. Gain control is performed in [pixel signal / for 1 horizontal line] parallel.

[0043]The column type analog to digital converter circuit 8 changes into a digital signal the pixel signal (analog signal) by which gain control was carried out in the column type auto gain controller circuit 7. Similarly, conversion to a digital signal is performed in [pixel signal / for 1 horizontal line] parallel.

[0044]The high luminance correction signal storing memory circuit 10 and especially the pixel signal storing memory circuit 11 are composition by which it is characterized in this embodiment. The pixel signal storing memory circuit 11 memorizes temporarily the predetermined pixel P and the pixel signal accumulated by the pixel P for 1 horizontal line in detail of the picture element region 2. Namely, the pixel signal for 1 horizontal line of the picture element region 2 is once memorized in 1 horizontal line memory circuit 6, This memorized pixel signal is transmitted through each of the column type auto gain controller circuit 7, the column type analog to digital converter circuit 8, and the high luminance correction signal storing memory circuit 10, and this pixel signal is memorized by the first rank of the pixel signal storing memory circuit 11. The pixel signal storing memory circuit 11 should just be provided with the capacity which can memorize the pixel signal for 1 horizontal line at least. It is preferred to equip the pixel signal storing memory circuit 11 with the capacity about several lines - tens of lines (for example, ten lines) according to the region of accommodation of a dynamic range practical. The pixel signal for 1 horizontal line memorized by the first rank of the pixel signal storing memory circuit 11 is transmitted to the next step, before the pixel signal for 1 horizontal line of the next step is transmitted from the picture element region 2. The pixel signal for 1 horizontal line which was transmitted to the final stage of the pixel signal storing memory circuit 11, and was memorized is outputted to the synthetic circuit 14 through the line selecting circuit 13, or is eliminated.

[0045]In the pixel signal storing memory circuit 11, transmission of the line writing direction of the pixel signal for 1 horizontal line is performed by the memory shift register circuit (MS circuit) 12. The pixel signal for specific 1 horizontal line is chosen by the line selecting circuit 13 among the pixel signals for 1 horizontal line transmitted to a line writing direction in the pixel signal storing memory circuit 11. The pixel signal for this specific selected 1 horizontal line is transmitted one by one to the synthetic circuit 14 by the horizontal shift register circuit 15 through the line selecting circuit 13.

[0046]Each storage cell of the pixel signal storing memory circuit 11 can transmit a pixel signal one by one, for example, is constituted from a memory cell of SRAM (Static Random Access Memory) by a flip-flop circuit and details. A memory cell is provided with the flip-flop circuit which comprises two p channel MISFET(s) for loads, and two n channel MISFET(s) for a drive, and two MISFET(s) for transmission, and is constituted.

[0047]The high luminance correction signal storing memory circuit 10 memorizes temporarily the same pixel P from which the pixel signal for 1 horizontal line which is chosen by the line selecting circuit 13 and

transmitted to the synthetic circuit 14 was taken out, and the high luminance correction signal accumulated by the same pixel P for 1 horizontal line in detail. The high luminance correction signal for 1 horizontal line as well as a pixel signal is once memorized in 1 horizontal line memory circuit 6, Through each of the column type auto gain controller circuit 7 and the column type analog to digital converter circuit 8, this memorized high luminance correction signal is transmitted to the high luminance correction signal storing memory circuit 10, and is memorized. The high luminance correction signal storing memory circuit 10 should just be provided with the capacity which can memorize the high luminance correction signal for 1 horizontal line at least. In this embodiment, each storage cell of the high luminance correction signal storing memory circuit 10 comprises a flip-flop circuit as well as the pixel signal storing memory circuit 11.

[0048]The high luminance correction signal memorized in the high luminance correction signal storing memory circuit 10 is transmitted one by one to the synthetic circuit 14 by the horizontal shift register circuit 15. The horizontal shift register circuit 15 is the same as the horizontal shift register circuit 15 used in the pixel signal storing memory circuit 11, and is made to serve a double purpose. That is, each of the pixel signal transmitted from the pixel signal storing memory circuit 11 and the high luminance correction signal transmitted from the high luminance correction signal storing memory circuit 10 is substantially transmitted to the synthetic circuit 14 by the same horizontal shift register circuit (one piece) 15 to the same timing.

[0049]Each of 1 horizontal line memory circuit 6, the column type auto gain controller circuit 7, the column type analog to digital converter circuit 8, the high luminance correction signal storing memory circuit 10, and the pixel signal storing memory circuit 11, Between the picture element region 2 and the horizontal shift register circuit 15, it is arranged in in-series.

[0050]The synthetic circuit 14 compounds the pixel signal transmitted through the line selecting circuit 13 from the pixel signal storing memory circuit 11, and the high luminance correction signal transmitted from the high luminance correction signal storing memory circuit 10, and generates the pixel signal with which high-intensity was amended. This pixel signal is amplified in the output amplifier circuit 16, and is outputted to the exterior of the solid state camera 1 through the external terminal (an outer lead or an outer pin) which is not illustrated from the output amplifier circuit 16.

[0051]The controller circuit 5 is connected to each of the vertical shift register circuits 3 and 4, the vertical shift register switch circuit 9, the horizontal shift register circuit 12, the memory shift register circuit 12, the line selecting circuit 13, and the synthetic circuit 16 (connection is omitted in part among drawing 1.), Operation of these peripheral circuits is controlled. A peripheral circuit is constituted by the subject in the complementary type MISFET in this embodiment.

[0052]The solid state camera 1 constituted in this way is closed by a resin sealed body or the ceramic sealed body (package), and is mounted on the wiring board of mounting devices, such as a camera.

[0053]Next, operation of the solid state camera 1 is explained. Drawing 3 is an important section expansion schematic diagram of the solid state camera 1 for explaining operation.

[0054]First, in the solid state camera 1, each of the pixel P(m-3) 1 arranged in one predetermined horizontal line of the picture element region 2, P(m-3)2, --, P(m-3) n is chosen. This selection is performed by choosing predetermined address signal line ADL in the vertical shift register circuit 3 and the vertical shift register switch circuit 9 which are shown in drawing 1 thru/or drawing 3. The pixel signal S for the selected pixel P(m-3) 1, P(m-3)2, --, 1 horizontal line from each of P(m-3) n is acquired. The pixel signal S is a signal acquired as a result of being accumulated by the long exposure time equivalent to a part for 1 frame period which

generates the picture of one sheet. Correctly, the pixel signal S is a signal acquired as a result of being accumulated by the exposure time which deducted the short exposure time (it is equivalent to several times - tens of times of the number of times of a horizontal scanning.) which generates a high luminance correction signal from the long exposure time equivalent to a part for 1 frame period.

[0055]The pixel signal S is once memorized through the video signal line 6L in 1 horizontal line memory circuit 6, This memorized pixel signal S is memorized by the first rank of the pixel signal storing memory circuit 11 through each of the column type auto gain controller circuit 7, the column type analog to digital converter circuit 8, and the high luminance correction signal storing memory circuit 10. The pixel signal S memorized by the first rank of the pixel signal storing memory circuit 11 is transmitted one by one to the storage cell of the next step by the memory shift register circuit 12. The transfer timing of the pixel signal S by the memory shift register circuit 12 synchronizes with the vertical-scanning timing of the vertical shift register circuit 3, and is controlled by the controller circuit 5.

[0056]If the pixel signal S for 1 horizontal line is taken out, the reset signal wire RSL will be chosen by the vertical shift register circuit 3 and the vertical shift register switch circuit 9 in the pixel P for this 1 horizontal line, and a reset action will be performed.

[0057]The controller circuit 5 chooses the pixel signal S (pixel signal for 1 horizontal line) memorized via the line selecting circuit 13 in the pixel signal storing memory circuit 11 after progress of the exposure time set up beforehand. For example, the pixel signal S which was transmitted to the 3rd step of the pixel signal storing memory circuit 11, and was memorized is chosen. This pixel signal S is transmitted to the synthetic circuit 14 through the line selecting circuit 13. Transmission of the pixel signal S to the synthetic circuit 14 is performed one by one by the horizontal shift register circuit 15.

[0058]Each of the pixel P(m-3) 1 which, on the other hand, took out the pixel signal S transmitted to this synthetic circuit 14, P(m-3)2, --, P(m-3) n is chosen again. This selection is performed by choosing predetermined address signal line ADL in the vertical shift register circuit 4 and the vertical shift register switch circuit 9 which are shown in drawing 1 thru/or drawing 3. The selected pixel P(m-3) 1, P(m-3)2, --, the high luminance correction signal Sy for 1 horizontal line are acquired from each of P(m-3) n. The high luminance correction signal Sy is a signal acquired as a result of being accumulated by the short exposure time after the pixel signal S was taken out and several times - tens of horizontal scannings were performed. If the high luminance correction signal Sy for 1 horizontal line is taken out, the reset signal wire RSL will be chosen by the vertical shift register circuit 4 and the vertical shift register switch circuit 9 in the pixel P for this 1 horizontal line, and a reset action will be performed.

[0059]The high luminance correction signal Sy is once memorized through the video signal line 6L in 1 horizontal line memory circuit 6, This memorized high luminance correction signal Sy is once memorized in the high luminance correction signal storing memory circuit 10 through each of the column type auto gain controller circuit 7 and the column type analog to digital converter circuit 8. The high luminance correction signal Sy once memorized in this high luminance correction signal storing memory circuit 10 is transmitted to the synthetic circuit 14. Transmission of the high luminance correction signal Sy to the synthetic circuit 14 is performed one by one by the horizontal shift register circuit 15. Transmission of the high luminance correction signal Sy is performed by the shared horizontal shift register circuit 15 synchronizing with the transfer timing of the pixel signal S.

[0060]In the synthetic circuit 14, the picture signal S and the high luminance correction signal Sy are

compounded, and pixel signal Sc by which high-intensity was amended is generated and outputted. Pixel signal Sc is amplified in the output amplifier circuit 16, and is outputted to the exterior of the solid state camera 1.

[0061]In the solid state camera 1 constituted in this way, the pixel signal S and the high luminance correction signal Sy are taken out from the same predetermined pixel P of the picture element region 2, the pixel signal S is memorized in the pixel signal storing memory circuit 11, and the high luminance correction signal Sy is memorized in the high luminance correction signal storing memory circuit 10. Since the high luminance correction signal storing memory circuit 10 is arranged between the picture element region 2 and the pixel signal storing memory circuit 11 and it is perpendicularly transmitted in order of the pixel signal S and the high luminance correction signal Sy, memory of the pixel signal S and memory of the high luminance correction signal Sy are performed to the same timing. Each of the pixel signal S and the high luminance correction signal Sy which were memorized is transmitted to the synthetic circuit 14 in the common horizontal shift register circuit 15. Therefore, since the horizontal shift register circuit to which only the high luminance correction signal Sy is transmitted becomes unnecessary and the common horizontal shift register circuit 15 is allocated in the pixel signal storing memory circuit 11 and the high luminance correction signal storing memory circuit 10, The number of horizontal shift register circuits can be reduced, and miniaturization of the solid state camera 1 and integration can be realized.

[0062]The synthetic circuit 14 is allocated in the solid state camera 1, and correction of the pixel signal S is made inside the solid state camera 1. That is, the pixel signal outputted from the solid state camera 1 will be one kind of pixel signal Sc by which high-intensity was amended. Therefore, since the number of external terminals of the solid state camera 1 is reducible, the miniaturization of the solid state camera 1 and integration (or reduction of package size) are realizable.

[0063]In the solid state camera 1, since regulation of the signal quantity of the high luminance correction signal Sy can carry out only by changing the selection part of the pixel signal storing memory circuit 11 in the line selecting circuit 13, it can carry out very simply. And since it can carry out substantially only by the solid state camera 1 side, regulation of the signal quantity of the high luminance correction signal Sy can be carried out very simply.

[0064]The pixel signal S acquired by the same predetermined pixel of the picture element region 2 in the solid state camera 1. Each of the high luminance correction signal Sy is serially transmitted to each of the high luminance correction signal storing memory circuit 10 and the pixel signal storing memory circuit 11 one by one, and extraction by the pixel signal S and the high luminance correction signal Sy by the synthetic circuit 14 is performed to the same timing. Therefore, since the circuit systems for compounding the pixel signal S and the high luminance correction signal Sy are reducible to 1 set, the miniaturization of the solid state camera 1 is realizable.

[0065]In the solid state camera 1, the circuit system for compounding the pixel signal S and the high luminance correction signal Sy as mentioned above can reduce to 1 set, and since one kind of output may be sufficient as pixel signal Sc by which high-intensity was amended, the data rate of pixel signal Sc is shortened (halved). The time which the output of the pixel signal for 1 frame period takes by shortening of the data rate of pixel signal Sc can be shortened, and the working speed of the solid state camera 1 can be accelerated.

[0066]

[Effect of the Invention]This invention reduces the number of external terminals, and can provide the solid state camera which can realize miniaturization and integration. Especially this invention realizes the miniaturization of a solid state camera, and can attain the miniaturization of mounting devices, such as a camera which mounts this solid state camera.

[0067]This invention reduces the data rates of a pixel signal, and can provide the solid state camera which can realize improvement in the speed of the output operation speed of a pixel signal.

[0068]This invention can adjust the signal quantity of a high luminance correction signal simply, and can provide the solid state camera which a dynamic range can control easily.

[Translation done.]